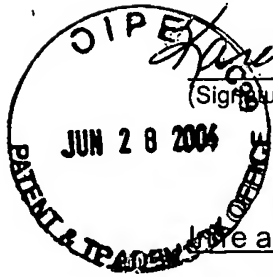


IFW

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to : Commissioner of Patents and Trademarks, Alexandria, VA.22313, on June 25 2004. The applicant and/or attorney requests the date of deposit as the filing date. Depositor: Karen Cinq-Mars



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Here application of _____:

June 25 2004

Chidambarao Dureseti et al.:

Group Art Unit: 2822

Serial No.10/605,167 :

Examiner: Lazena Martin

Filed: 9/12/2003 :

International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: Mosfet Performance Improvement Using Deformation in SOI Structure

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

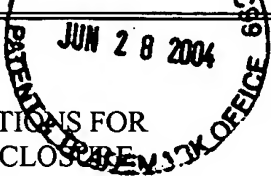
Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Chidambarao Dureseti et al.

By Joseph P. Abate 6-25-04
Joseph P. Abate, Attorney
Registration No. 30,238
Telephone No. 845-894-4633

FORM PTO-1449 (Modified)				ATTY. DOCKET NO. FIS920030185US1	SERIAL NO. 10/605/167
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		APPLICANT: Dureseti Chidambarao, et al.			
(Use several sheets if necessary)		FILING DATE: 9/12/03		GROUP: 2822	

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6,228,694 B1	5/8/2001	Doyle et al.			
	6,406,973 B1	6/18/2002	Lee			
	6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
	6,368,931 B1	4/9/2002	Kuhn, et al.			
	5,310,446	5/10/94	Konishi et al.			
	4,853,076	8/1/89	Tsaur et al.			
	US 2002/0090791 A1	7/11/2002	Doyle et al.			
	US 2002/0074598 A1	6/20/2002	Doyle et al.			
	6,509,618 B2	7/21/2003	Jan et al.			
	6,476,462 B2	11/5/2002	Shimizu et al.			
	6,362,082 B1	3/26/2002	Doyle et al.			
	6,228,694 B1	5/8/2001	Doyle et al.			
	5,565,697	10/15/96	Asakawa et al.			
	US 2003/0040158 A1	2/27/2003	Saitoh			
	US 2002/0086472 A1	7/4/2002	Roberds et al.			
	6,521,964 B1	2/18/2003	Jan et al.			
	6,506,652	01/14/03	Jan, et al.			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER

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REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS				
EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		5,081,513	1/14/1992	Jackson, et al.			
		3,602,841	8/31/1971	McGroddy			
		6,531,740	3/11/2003	Bosco, et al.			
		6,531,369	3/11/2003	Ozkan, et al.			
		6,501,121	12/31/2002	Yu, et al.			
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		6,493,497	12/10/2002	Ramdani, et al.			
		6,403,975	6/11/2002	Brunner, et al.			
		6,361,885	3/26/2002	Chou			
		6,255,169	7/3/2001	Li, et al.			
		6,246,095	6/12/2001	Brady, et al.			
		6,165,383	12/26/2000	Chou			
		6,133,071	10/17/2000	Nagai			
		6,046,464	4/4/2000	Schetzina			
		6,025,280	2/15/2000	Brady, et al.			

FOREIGN PATENT DOCUMENTS								
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	5,940,736	8/17/1999	Brady, et al.			
	5,880,040	3/9/1999	Sun, et al.			
	5,861,651	1/19/1999	Brasen, et al.			
	5,679,965	10/21/1997	Schetzina			
	5,670,798	9/23/1997	Schetzina			
	5,561,302	10/1/1996	Candelaria			
	5,471,948	12/5/1995	Burroughes, et al.			
	5,459,346	10/17/1995	Asakawa, et al.			
	5,391,510	2/21/1995	Hsu, et al.			
	5,371,399	12/6/1994	Burroughes, et al.			
	5,108,843	4/28/1992	Ohtaka, et al.			
	5,060,030	10/22/1991	Hoke			
	4,958,213	9/18/1990	Eklund, et al.			
	4,665,415	5/12/1987	Esaki, et al.			

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		5,989,978	11/23/1999	Peidous			
		6,284,626	9/4/2001	Kim			
		6,274,444	8/14/2001	Wang			
		6,261,964	7/17/2001	Wu, et al.			
		6,221,735	4/24/2001	Manley, et al.			
		6,117,722	9/12/2000	Wuu, et al.			
		6,107,143	8/22/2000	Park, et al.			
		6,090,684	7/18/2000	Ishitsuka, et al.			
		6,066,545	5/23/2000	Doshi, et al.			
		6,008,126	12/28/1999	Leedy			
		5,946,559	8/31/1999	Leedy			
		5,840,593	11/24/1998	Leedy			
		5,592,018	1/7/1997	Leedy			
		5,592,007	1/7/1997	Leedy			
		5,571,741	11/5/1996	Leedy			

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	5,557,122	9/17/1996	Shrivastava, et al.			
	5,354,695	10/11/1994	Leedy			
	5,134,085	7/28/1992	Gilgen, et al.			
	5,006,913	4/9/1991	Sugahara, et al.			
	4,952,524	8/28/1990	Lee, et al.			
	4,855,245	8/8/1989	Neppl, et al.			

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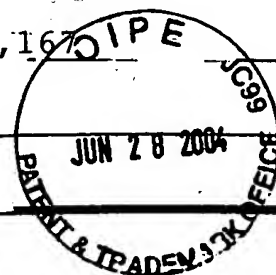
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LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S
INFORMATION DISCLOSURE STATEMENT

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Page 1 of 1

Attorney Docket No.:
FIS920030 185Serial No.:
10/605,167Applicant:
Chidambarrao Dureseti et al.Filing Date:
9/12/03Group:
2822

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

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		Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
		Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
		Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
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		A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
		K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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